Application No.: 10/713,652 Docket No.: 03226/351001; SUN040253

AMENDMENTS TO THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) A method for tracing on a processor comprising:

executing an execution control block on the processor to obtain data, wherein an interrupt on the processor is disabled prior to executing the execution control block and the interrupt is enabled after execution of the execution control block is completed;

storing the data in a first buffer, wherein the first buffer is set to active; and

setting the first buffer to inactive and setting a second buffer to active, wherein the interrupt on the processor is disabled prior to switching the first buffer to inactive and the interrupt is enabling after setting the second buffer to active,

wherein executing the execution control block to obtain data and switching an active status between the first buffer and the second buffer are mutually exclusively performed using the processor,

wherein the execution control block comprises an enabled probe identification identifying an action defining the data to be obtained from a probe in an instrumented program, and

wherein a stored data set size is determined during buffering using the enabled probe identification.

2. (Currently Amended) The method of claim 1, further comprising:

triggering [[a]] the probe in [[an]] the instrumented program; and

determining the execution control block associated with the probe.

3. (Original) The method of claim 2, further comprising:

associating the probe with a probe identifier.

4. (Previously Presented) The method of claim 3, wherein the determining the execution control block associated with the probe comprises querying a global array.

5. (Original) The method of claim 4, wherein the probe identifier is used to query the global array.

6. (Original) A method of claim 3, further comprising:

associating the execution control block to the probe identifier.

7. (Currently Amended) The method of claim 1, wherein the execution control block further comprises:

a predicate defining criterion for executing the execution control block; and

a consumer state component defining information associated with a consumer~~; and~~

~~an action defining the data to be obtained from the instrumented program at the probe~~.

8. (Original) The method of claim 5, wherein the execution control block is an element in a linked list.

9. (Original) The method of claim 6, wherein the execution control block further comprises:

a pointer to a next execution control block.

10. (Original) The method of claim 7, wherein the first buffer and the second buffer are associated with the consumer.

11. (Previously Presented) The method of claim 10, wherein switching the first buffer to inactive and setting the second buffer to active comprises:

searching for the first buffer and the second buffer associated with the consumer using the consumer state component.

12. (Original) The method of claim 1, wherein setting the first buffer to inactive and setting the second buffer to active occurs at a preset interval.

13. (Currently Amended) A system for tracing, comprising:

a processor;

a first buffer associated with the processor, wherein the first buffer is set to active;

a second buffer associated with the processor, wherein the second buffer is set to inactive;

an execution control block comprising an enabled probe identification identifying an action defining data to be obtained from a probe in an instrumented program, ~~associated with a probe configured to obtain data from the probe~~, wherein an interrupt on the processor is disabled prior to executing the execution control block and the interrupt on the processor is enabled after execution of the execution control block is completed; and

a tracing framework configured to store the data in the first buffer and configured to set the first buffer to inactive and the second buffer to active, wherein the tracing framework is configured to issue a cross-call prior to setting the first buffer to inactive and the second buffer to active,

wherein executing the execution control block on the processor to obtain data and switching an active status between the first buffer and the second buffer are mutually exclusively performed using the processor, and

wherein a stored data set size is determined during buffering using the enabled probe identification.

14. (Canceled)

15. (Original) The system of claim 13, further comprising:

a consumer associated with the first buffer and the second buffer.

16. (Original) The system of claim 13, wherein the cross-call comprises disabling an interrupt on the processor prior to setting the first buffer to inactive and enabling the interrupt after setting the second buffer to active.

17. (Original) The system of claim 13, wherein the tracing framework is configured to disable an interrupt prior to obtaining data from the probe and enable the interrupt after obtaining data from the probe.

18. (Currently Amended) The system of claim 13, wherein the execution control block further comprises:

a predicate defining criterion for executing the execution control block; and

a consumer state component defining information associated with a consumer; and

~~an action defining the data to be obtained from the instrumented program at the probe.~~

19. (Currently Amended) The system of claim 18, wherein the tracing framework is configured to obtain the execution control block ~~associated with the probe~~ using ~~a~~ the consumer state component.

20. (Original) The system of claim 13, wherein the first buffer comprises a drop count.

21. (Currently Amended) A network system having a plurality of nodes, comprising:

a processor;

a first buffer associated with the processor, wherein the first buffer is set to active;

a second buffer associated with the processor, wherein the second buffer is set to inactive;

an execution control block comprising an enabled probe identification identifying an action defining data to be obtained from a probe in an instrument program, ~~associated with a probe configured to obtain data from the probe,~~ wherein an

interrupt on the processor is disabled prior to executing the execution control block and the interrupt on the processor is enabled after execution of the execution control block is completed; and

a tracing framework configured to store the data in the first buffer and configured to set the first buffer to inactive and the second buffer to active, wherein the tracing framework is configured to issue a cross-call prior to setting the first buffer to inactive and the second buffer to active,

wherein executing the execution control block on the processor to obtain data and switching an active status between the first buffer and the second buffer are mutually exclusively performed using the processor,

wherein a stored data set size is determined during buffering using the enabled probe identification,

wherein the processor executes on any node of the plurality of nodes,

wherein the first buffer executes on any of the plurality of nodes,

wherein the second buffer executes on any of the plurality of nodes,

wherein the execution control block executes on any of the plurality of nodes, and

wherein the tracing framework executes on any of the plurality of nodes.

22. (Previously Presented) The network system of claim 21, wherein the cross-call comprises disabling an interrupt on the processor prior to setting the first buffer to inactive and enabling the interrupt after setting the second buffer to active.

23. (Currently Amended) The network system of claim 21, wherein the execution control block further comprises:

a predicate defining criterion for executing the execution control block; and

a consumer state component defining information associated with a consumer~~; and an action defining the data to be obtained from the instrumented program at the probe~~.

--End Examiner's Amendment--

Allowable Subject Matter

4. Claims 1-13 and 15-23 are allowed.

5. The following is an examiner's statement of reasons for allowance: The examiner indicated that this application would be in condition for allowance if the independent claims 1, 13, and 21 are amended to include the features of "wherein the execution control block comprises an enabled probe identification identifying an action defining the data to be obtained from a probe in an instrumented program, and wherein a stored data set size is determined during buffering using the enabled probe identification." The above features, taken in combination with all remaining features of the independent claim are not taught or suggested by the prior art of record. The applicant agreed to amend the independent claims 1, 13, and 21 as indicated by the examiner. The distinctions provided by the independent claims apply equally to all dependent claims. Thus all pending claims 1-13 and 15-23 are allowed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to J. Derek Rutten whose telephone number is (571)272-3703. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571)272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

jdr

TUAN DAM
SUPERVISORY PATENT EXAMINER

Application No.: 10/713,652 Docket No.: 03226/351001; SUN040253

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storing the data in a first buffer, wherein the first buffer is set to active; and

setting the first buffer to inactive and setting a second buffer to active, wherein the interrupt on the processor is disabled prior to switching the first buffer to inactive and the interrupt is enabling after setting the second buffer to active,

wherein executing the execution control block to obtain data and switching an active status between the first buffer and the second buffer are mutually exclusively performed using the processor,

wherein the execution control block comprises an enabled probe identification identifying an action defining the data to be obtained from a probe in an instrumented program, and

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2. (Currently Amended) The method of claim 1, further comprising:

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determining the execution control block associated with the probe.

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4. (Previously Presented) The method of claim 3, wherein the determining the execution control block associated with the probe comprises querying a global array.

5. (Original) The method of claim 4, wherein the probe identifier is used to query the global array.

6. (Original) A method of claim 3, further comprising:

associating the execution control block to the probe identifier.

7. (Currently Amended) The method of claim 1, wherein the execution control block further comprises:

a predicate defining criterion for executing the execution control block; and

a consumer state component defining information associated with a consumer~~; and~~

~~an action defining the data to be obtained from the instrumented program at the probe~~.

8. (Original) The method of claim 5, wherein the execution control block is an element in a linked list.

9. (Original) The method of claim 6, wherein the execution control block further comprises:

a pointer to a next execution control block.

10. (Original) The method of claim 7, wherein the first buffer and the second buffer are associated with the consumer.

11. (Previously Presented) The method of claim 10, wherein switching the first buffer to inactive and setting the second buffer to active comprises:

searching for the first buffer and the second buffer associated with the consumer using the consumer state component.

12. (Original) The method of claim 1, wherein setting the first buffer to inactive and setting the second buffer to active occurs at a preset interval.

13. (Currently Amended) A system for tracing, comprising:

a processor;

a first buffer associated with the processor, wherein the first buffer is set to active;

a second buffer associated with the processor, wherein the second buffer is set to inactive;

an execution control block comprising an enabled probe identification identifying an action defining data to be obtained from a probe in an instrumented program, ~~associated with a probe configured to obtain data from the probe,~~ wherein an interrupt on the processor is disabled prior to executing the execution control block and the interrupt on the processor is enabled after execution of the execution control block is completed; and

a tracing framework configured to store the data in the first buffer and configured to set the first buffer to inactive and the second buffer to active, wherein the tracing framework is configured to issue a cross-call prior to setting the first buffer to inactive and the second buffer to active,

wherein executing the execution control block on the processor to obtain data and switching an active status between the first buffer and the second buffer are mutually exclusively performed using the processor, and

wherein a stored data set size is determined during buffering using the enabled probe identification.

14. (Canceled)

15. (Original) The system of claim 13, further comprising:

a consumer associated with the first buffer and the second buffer.

16. (Original) The system of claim 13, wherein the cross-call comprises disabling an interrupt on the processor prior to setting the first buffer to inactive and enabling the interrupt after setting the second buffer to active.

17. (Original) The system of claim 13, wherein the tracing framework is configured to disable an interrupt prior to obtaining data from the probe and enable the interrupt after obtaining data from the probe.

18. (Currently Amended) The system of claim 13, wherein the execution control block further comprises:

a predicate defining criterion for executing the execution control block; and

a consumer state component defining information associated with a consumer~~; and~~

~~an action defining the data to be obtained from the instrumented program at the probe~~.

19. (Currently Amended) The system of claim 18, wherein the tracing framework is configured to obtain the execution control block ~~associated with the probe~~ using a the consumer state component.

20. (Original) The system of claim 13, wherein the first buffer comprises a drop count.

21. (Currently Amended) A network system having a plurality of nodes, comprising:

a processor;

a first buffer associated with the processor, wherein the first buffer is set to active;

a second buffer associated with the processor, wherein the second buffer is set to inactive;

an execution control block comprising an enabled probe identification identifying an action defining data to be obtained from a probe in an instrument program, ~~associated with a probe configured to obtain data from the probe,~~ wherein an

interrupt on the processor is disabled prior to executing the execution control block and the interrupt on the processor is enabled after execution of the execution control block is completed; and

a tracing framework configured to store the data in the first buffer and configured to set the first buffer to inactive and the second buffer to active, wherein the tracing framework is configured to issue a cross-call prior to setting the first buffer to inactive and the second buffer to active,

wherein executing the execution control block on the processor to obtain data and switching an active status between the first buffer and the second buffer are mutually exclusively performed using the processor,

wherein a stored data set size is determined during buffering using the enabled probe identification,

wherein the processor executes on any node of the plurality of nodes,

wherein the first buffer executes on any of the plurality of nodes,

wherein the second buffer executes on any of the plurality of nodes,

wherein the execution control block executes on any of the plurality of nodes, and

wherein the tracing framework executes on any of the plurality of nodes.

22. (Previously Presented) The network system of claim 21, wherein the cross-call comprises disabling an interrupt on the processor prior to setting the first buffer to inactive and enabling the interrupt after setting the second buffer to active.

23. (Currently Amended) The network system of claim 21, wherein the execution control block further comprises:

a predicate defining criterion for executing the execution control block; and

a consumer state component defining information associated with a consumer~~; and an action defining the data to be obtained from the instrumented program at the probe~~.